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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,859	04/14/2004	Hee-Cheol Choi	SAM-0522	6192

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EXAMINER	
MISLEH, JUSTIN P	
ART UNIT	PAPER NUMBER
2622	
MAIL DATE	DELIVERY MODE
04/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,859	CHOI, HEE-CHEOL	
	Examiner	Art Unit	
	JUSTIN P. MISLEH	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 1, 2008 has been entered.

Response to Arguments

2. Applicant's arguments with respect to **Claims 1 – 50** have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1 – 50** are rejected under 35 U.S.C. 103(a) as being unpatentable over Itani et al. (US 6,650,364 B1) in view Parks (US 6,838,787 B2).

Claim 15 is an apparatus claim and is identical to a combination of apparatus Claims 1 and 7. Likewise, Claim 40 is a method claim and is identical to a combination of method Claims

26 and 32. Finally, Claims 1, 7, 15 and Claims 26, 32, and 40 are corresponding apparatus and method claims, respectively. Accordingly, they will be rejected together using the claim language of the apparatus claims.

5. For **Claims 1, 7, 15, 26, 32, and 40**, Itani et al. disclose, as shown in figures 1A and 1B, an image processing system, comprising:

a correlated double sampler (CDS) for receiving an input signal (114), sampling the input signal and providing an output signal (see figure 1C), the CDS (114) comprising an amplifier (130) for amplifying the input signal (Vin) and a variable capacitance unit (C3 and C4) having first (C3) and second (C4) variable input capacitances, and a programmable gain amplifier (PGA) for receiving the output signal from the CDS (114) and amplifying the received signal (117).

Itani et al. does not teach wherein the first (C3) variable input capacitance being connected to a first input of the amplifier and the second (C4)variable input capacitance being connected to a second input of the amplifier.

On the other hand, Parks also discloses an image processing system including a CDS. More specifically, Parks discloses, as shown in figure 3, a CDS including an amplifier (90), where the amplifier includes two inputs (Vout A and Vout B). Parks further discloses where each of the amplifier inputs (Vout A and Vout B) is connected to a respective variable input capacitance (70a and 70b).

Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included a first variable input capacitance being connected to a first input of the amplifier and a second variable input capacitance being connected to a second

input of the amplifier (as taught by Park) in the image processing system (disclosed by Itani et al.) for the advantage of *providing an image processing system that permits the CDS noise performance to be optimized for more than one frequency* (see Parks, column 1, lines 38 – 40).

6. As for **Claims 8, 19, 33, and 44**, Itani et al. discloses, as shown in figures 4 and 5D, wherein a gain in the PGA is settable to one of a plurality of levels.

7. As for **Claims 9, 20, 34, and 45**, Itani et al. discloses, as shown in figures 4 and 5D, wherein a gain in the PGA is settable to a level between 1.0 and 2.0 (Figure 4 shows the PGA is capable of being set at 0 db, or unity gain).

8. As for **Claims 5, 10, 21, 30, 35, and 46**, Itani et al. discloses, as shown in figure 5B, wherein a gain in the CDS (114) and a gain in the PGA are settable by a digital input signal (see "Gain Code" in figure 5B).

9. As for **Claims 6, 11, 22, 31, 36, and 47**, Itani et al. discloses, as shown in figure 5A, wherein the digital input signal contains a plurality of bits (at least 11 bits; see output of 196 in figure 5A).

10. As for **Claims 12, 23, 37, and 48**, Itani et al. discloses, as shown in figure 5B, wherein a first portion of the bits is applied to the CDS to set gain in the CDS and a second portion of the bits is applied to the PGA to set gain in the PGA (see column 6, lines 53 – 50).

11. As for **Claims 13, 24, 38, and 49**, Itani et al. discloses, as shown in figure 5B, wherein an overall gain of the system comprises a combination of gain in the CDS and gain in the PGA (see column 6, lines 53 – 50).

12. As for **Claims 14, 25, 39, and 50**, Itani et al. discloses, as shown in figure 4, wherein the overall gain is pseudo-logarithmic.

13. As for **Claims 2, 16, 27, and 41**, Itani et al. discloses, as shown in figures 4 and 5D, wherein a gain in the CDS is settable to one of a plurality of levels.

14. As for **Claims 3, 17, 28, and 42**, Park discloses, as shown in figure 5, wherein a gain in the CDS is settable to at least one of an N number of levels (An N number of levels includes four levels).

15. As for **Claims 4, 18, 29, and 43**, Itani et al. discloses, as shown in figures 4 and 5D, wherein a gain in the CDS is settable to a level between 1.0 and 2.0 (Figure 4 shows the CDS is capable of being set at 0 db, or unity gain).

Cited Prior Art

16. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure for the following reasons:

- **Fujimoto ('241)** discloses an image processing circuit that sets a gain of a CDS to one of three levels and digitally sets a gain of a PGA to one of a plurality of levels.
- **Rogers et al. ('720)** discloses an image processing circuit that digitally sets a gain of a PGA to one of a plurality of levels.
- **Lee ('364)** discloses amplifier gain controller using switched unit capacitances.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Lin Ye can be reached on 571.272.7372. The fax phone number for the organization where this application or proceeding is assigned is 571.273.8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Justin P. Misleh/
Examiner, GAU 2622
April 23, 2008